(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 717 341 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
19.06.1996 Bulletin 1996/25

(51) Int Cl.[6]: **G06F 1/26**, G06K 7/00

(21) Application number: **95308416.7**

(22) Date of filing: **23.11.1995**

(84) Designated Contracting States:
DE FR GB

(30) Priority: **15.12.1994 JP 311419/94**

(71) Applicant: **INTERNATIONAL BUSINESS MACHINES CORPORATION**
Armonk, NY 10504 (US)

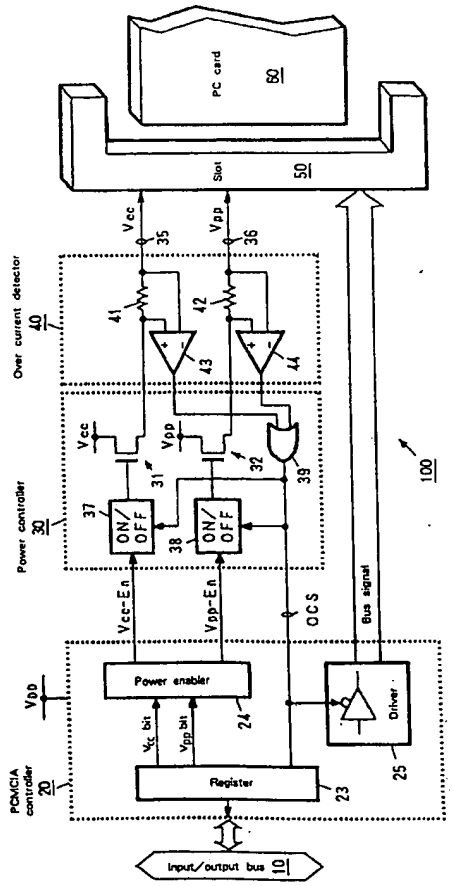
(72) Inventors:
- **Yuzawa, Shigeru**
  Yamato-shi, Kanagawa-ken (JP)
- **Karube, Satoshi**
  Kamakura-shi, Kanagawa-ken (JP)

(74) Representative: **Williams, Julian David**
IBM United Kingdom Limited,
Intellectual Property Department,
Hursley Park
Winchester, Hampshire SO21 2JN (GB)

(54) Power enabling apparatus and method

(57) Disclosed is an input/output device controller for securely supplying power to a PC card that is loaded into a slot of a personal computer. The input/output device controller, which permits an information processing apparatus to communicate with an input/output device, comprises: an interface that is employed for data exchange with the input/output bus of the information processing apparatus, a register for temporarily holding part of a data group that is to be exchanged, a driver for transmitting a signal to the input/output device, a power enabler for, in consonance with the contents written in the register, connecting/disconnecting a power line that joins the input/output device to a power source, and detection means for detecting an over current across the power line; and writes in the register the detection result and renders off the driver in response to the detection result. when an abnormality is detected in the supply of power to the PC card, the detection result can be reported to the PC. In addition, when an abnormality in the supply of power to the PC card is detected, the output of the driver for transmitting a signal to the PC card is halted, and the destruction of the internal circuit of the PC card due to the latch-up can be prevented.

FIG. 1



EP 0 717 341 A1

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 717 341 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
19.06.1996 Bulletin 1996/25

(51) Int Cl.[6]: **G06F 1/26**, G06K 7/00

(21) Application number: **95308416.7**

(22) Date of filing: **23.11.1995**

(84) Designated Contracting States:
DE FR GB

(30) Priority: **15.12.1994 JP 311419/94**

(71) Applicant: **INTERNATIONAL BUSINESS MACHINES CORPORATION**
Armonk, NY 10504 (US)

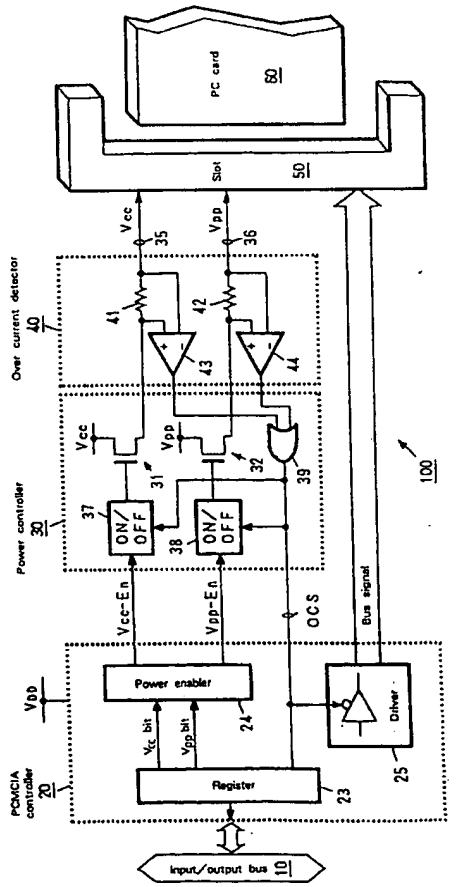
(72) Inventors:
- **Yuzawa, Shigeru**
  Yamato-shi, Kanagawa-ken (JP)
- **Karube, Satoshi**
  Kamakura-shi, Kanagawa-ken (JP)

(74) Representative: **Williams, Julian David**
IBM United Kingdom Limited,
Intellectual Property Department,
Hursley Park
Winchester, Hampshire SO21 2JN (GB)

(54) Power enabling apparatus and method

(57) Disclosed is an input/output device controller for securely supplying power to a PC card that is loaded into a slot of a personal computer. The input/output device controller, which permits an information processing apparatus to communicate with an input/output device, comprises: an interface that is employed for data exchange with the input/output bus of the information processing apparatus, a register for temporarily holding part of a data group that is to be exchanged, a driver for transmitting a signal to the input/output device, a power enabler for, in consonance with the contents written in the register, connecting/disconnecting a power line that joins the input/output device to a power source, and detection means for detecting an over current across the power line; and writes in the register the detection result and renders off the driver in response to the detection result. when an abnormality is detected in the supply of power to the PC card, the detection result can be reported to the PC. In addition, when an abnormality in the supply of power to the PC card is detected, the output of the driver for transmitting a signal to the PC card is halted, and the destruction of the internal circuit of the PC card due to the latch-up can be prevented.

FIG. 1



EP 0 717 341 A1

quently loaded into and unloaded from a PC, and various PC card types that are produced by many makers are now commercially available. However, almost nothing concerning the consumption of power by PC cards is contained in the current standards that are specified for PC cards. There are PC cards that have a large power consumption that exceeds the power supply capabilities of the PC card power circuits that are provided in the PCs, and there have been some instances where such PC cards have been loaded into the slots 50 of PCs. In another cases, the power sources are short-circuited to the GND because of the abnormalities of internal circuits of the PC cards. Further, since the present I/O card standards that were specified for PC cards were added to the original standards that were specified for memory cards, cards such as hard disk cards (the so-called Type III), whose power consumption is large (which is neither abnormal nor over current), have been loaded into slots that were intended for memory cards. When the power consumption of a loaded PC card is unexpectedly great, the PC card power supply circuit in the PC and the power circuit of the PC itself will be destroyed, and the data contents of the memory for the PC will be lost.

In short, there are no established standards that cover power consumption by PC cards, and the internal state of PC cards cannot be determined at a glance. As, in spite of these problems, frequent active insertion, and extraction, of PC cards occurs as a consequence of the principle of Plug and Play, power protection countermeasures for PC cards are very important.

To provide a secure supply of power for PC cards, conventionally, over current protection circuits are located on the power lines. Fuses 33 and 34 that are inserted in series on the power lines 35 and 36 in Fig. 11 are equivalent to such circuits. However, over current protection that involves the use of fuses has the following problems.

(1) Generally, the fuses 33 and 34 that are employed for the power controller 30 are chip types that are assembled on a board by soldering, and replacing them is not easy, even if they can be cut off. Accordingly, once the fuses have blown, even when a normal PC card is loaded to the slot, the PC card is not activated.

(2) Generally, the fuses are components that have a low response speed, so that over current flows to the PC card for a moment until the fuses are blown. As an excess current flows to the PC card and the voltage within the PC is reduced, the operation of the PC may be halted and the contents of the main memory may be damaged.

(3) When the PC card is not activated because the PC card causes the fuses to blow, there is no interface, specified by PCMCIA/JEIDA, which can report the cause of the fault to a user or to the PC. Since the user is not aware of the abnormality, in many cases he inserts the PC card, which contains the abnormality, into other slots on the same PC or another PC, one after another, to try to determine what is wrong. This is more often performed with PC cards for which detachment is made easier for Plug and Play purposes. The repetitious attempts to determine what is wrong may cause the fuses of every PC card slot to be blown. Further, since the driver for the PCMCIA controller is maintained in the ON state while there is no power supplied to the PC card, the PC, to which the abnormality is not reported, will try to access the PC card. However, since the circuit components, such as transistors, can switch the input signal properly only upon the application of a drive voltage, and can not be activated when no drive voltage is applied, a current may flow in an unexpected direction within the components or between the components. As a result, some signals may cause a large current to sink, and the internal circuit of the PC card may be destroyed by the latch-up. When the fuses have blown only on the V_{CC} side, only the voltage V_{PP} is available to drive the PC card. The application of only the voltage V_{PP}, which is originally optional, is counter to the specifications and creates a dangerous condition for PC cards.

There is one method where information concerning the power consumption of the PC card is written, as part of the card attribute information (CIS), into an internal ROM on the PC card so that the PC can read that information. However, as power must be supplied to the PC card in order for the information to be read from the ROM, this method does not provide complete protection.

As is described above, when a power abnormality occurs on a PC card, it is imperative that the supply of power be halted before the PC is damaged and that information concerning the occurrence of the abnormality be transmitted to the system of the PC.

In accordance with the present invention there is now provided apparatus for controlling a supply of power by an information processing system to a detachable input/output device, comprising: a first power line for supplying power at a first voltage level; a second power line for supplying power at a second voltage level; a first detector for detecting an over current across the first power line; a second detector for detecting an over current across the second power line; OR means for logically adding the outputs of both the first and second detectors; a first switch that is employed for connection and disconnection of the first power line in response to an output of the OR means; and a second switch that is employed for connection and disconnection of the second power line in response to an output of the OR means.

Viewing another aspect of the present invention, there is now provided an input/output device controller, which permits an information processing apparatus to communicate with a detachable input/output device, comprising: an interface that is employed for data exchange with an input/output bus of the information processing apparatus, a register for temporarily holding part of a data group that is to be exchanged, a driver for transmitting a signal to the input/output device, a power enabler for, in accordance with data that are written into the register, connecting/disconnecting a power line that joins the input/output device to a power source, detection means for detecting an over current across the power line; and rendering off the driver in response to the detection result that is obtained by the detection means.

Viewing yet another aspect of the present invention, there is now provided a power enabling method, for controlling a supply of power by an information processing apparatus to a detachable input/output device, comprising the steps of: detecting whether or not there exists a supplied power abnormality; halting the supply of power in response to detection of the abnormality; halting transmission of a signal to the input/output device in response to the detection of the abnormality; and reporting the detection of the abnormality to the information processing apparatus.

The present invention this provides a power enabling mechanism, a power enabling method, and an input/output device controller for controlling a supply of power by an information processing apparatus to an input/output device that is loaded into it.

The input/output device may, for example, be a PC card that is loaded into a slot of a personal computer (PC).

In preferred embodiments of the present invention there is provided a power enabling mechanism, a power enabling method, and an input/output device controller for securely supplying power to a PC card that is loaded into a slot of a personal computer, and for preventing a voltage reduction and a circuit fault of the PC and the latch-up of the PC card even when power consumption by the PC card is abnormal (or a large power consumption exceeds specified standards).

In one preferred embodiment of the present invention, a power enabling mechanism, which controls a supply of power by an information processing apparatus to a detachable input/output device, comprises: a first power line for supplying power at a first voltage level; a second power line for supplying power at a second voltage level; a first detector for detecting an over current across the first power line; a second detector for detecting an over current across the second power line; OR means for logically adding the outputs of the first and the second detectors; a first switch that is employed for connection and disconnection of the first power line in response to an output of the OR means; and a second switch that is employed for connection and disconnection of the second power line in response to an output of the OR means.

In another preferred embodiment of the present invention, a power enabling mechanism, which controls a supply of power by an information processing apparatus to a detachable input/output device, comprises: a first power line for supplying power at a first voltage level, a second power line for supplying power at a second voltage level, a first detector for detecting an over current across the first power line, a second detector for detecting an over current across the second power line, OR means for logically adding the outputs of the first and the second detectors, a first switch that is employed for connection and disconnection of the first power line in response to an output of the OR means, a second switch that is employed for connection and disconnection of the second power line in response to an output of the OR means; and employs the OR means also to report the output to the information processing apparatus.

In yet another preferred embodiment of the present invention, a power enabling mechanism, which controls a supply of power by an information processing apparatus to a detachable input/output device, comprises: a first power line for supplying power at a first voltage level; a second power line for supplying power at a second voltage level; a first fuse that blows when an over current flows across the first power line; a second fuse that blows when an over current flows across the second power line; a first detection line that is set to the ON state by the blowing of the first fuse; a second detection line that is set to the ON state by the blowing of the second fuse; and a report line that is employed to carry a notice to the information processing apparatus when at least one of the first and the second detection lines is set in the ON state.

In still another preferred embodiment of the present invention, an input/output device controller, which permits an information processing apparatus to communicate with a detachable input/output device, comprises: an interface that is employed for data exchange with an input/output bus of the information processing apparatus, a register for temporarily holding part of a data group that is to be exchanged, a driver for transmitting a signal to the input/output device, a power enabler for, in consonance with data that are written into the register, connecting/disconnecting a power line that joins the input/output device to a power source, detection means for detecting an over current across the power line; and renders off the driver in response to the detection result that is obtained by the detection means.

In a further preferred embodiment of the present invention, an input/output device controller, which permits an information processing apparatus to communicate with a detachable input/output device, comprises: an interface that is employed for data exchange with an input/output bus of the information processing apparatus, a register for temporarily holding part of a data group that is to be exchanged, a driver for transmitting a signal to the input/output device, a power enabler for, in con-

sonance with the contents written in the register, connecting/disconnecting a power line that joins the input/output device to a power source, detection means for detecting an over current across the power line; and provides in the register a field in which the detection result is written and renders off the driver in response to the detection result that is obtained by the detection means.

In an example of the present invention, a power enabling method, for controlling a supply of power by an information processing apparatus to a detachable input/output device, comprises the steps of: detecting whether or not there exists a supplied power abnormality; and halting transmission of a signal to the input/output device in response to the abnormality that is detected.

In another example of the present invention, a power enabling method, for controlling a supply of power by an information processing apparatus to a detachable input/output device, comprises the steps of: detecting whether or not there exists a supplied power abnormality; halting the supply of power in response to detection of the abnormality; halting transmission of a signal to the input/output device in response to the detection of the abnormality; and reporting the detection of the abnormality to the information processing apparatus.

In yet another example of the present invention, a power enabling method, for controlling a supply of power by an information processing apparatus to a detachable input/output device, comprises the steps of: initiating the supply of power in response to the loading of the input/output device into the information processing apparatus; detecting whether or not there exists a supplied power abnormality; halting the supply of power in response to detection of the abnormality; halting transmission of a signal to the input/output device in response to the detection of the abnormality; reporting the detection of the abnormality to the information processing apparatus; and maintaining the halting of the supply of power to the input/output device at least while the input/output device is loaded.

In still another example of the present invention, a power enabling mechanism, which controls a supply of power by an information processing apparatus to a detachable input/output device, comprises: a first power line for supplying power at a first voltage level; a second power line for supplying power at a second voltage level; a first detector for detecting an over current across the first power line; a second detector for detecting an over current across the second power line; OR means for logically adding the outputs of the first and the second detectors; a first switch that is employed for connection and disconnection of the first power line; first ON/OFF control means for rendering on the first switch according to an instruction from the information processing apparatus and for rendering off the first switch in response to the logical sum that is acquired by the OR means and maintaining an OFF state until an instruction is received from the information processing apparatus; a second switch that is employed for connection and disconnection of the second power line; and second ON/OFF control means for rendering on the second switch according to an instruction from the information processing apparatus and for rendering off the second switch in response to the logical sum that is acquired by the OR means and maintaining an OFF state until an instruction is received from the information processing apparatus.

In a further example of the present invention, a power enabling mechanism, which controls a supply of power by an information processing apparatus to a detachable input/output device, comprises: a first power line for supplying power at a first voltage level, a second power line for supplying power at a second voltage level, a first detector for detecting an over current across the first power line, a second detector for detecting an over current across the second power line, OR means for logically adding the outputs of the first and the second detectors, a first switch that is employed for connection and disconnection of the first power line, first ON/OFF control means for rendering on the first switch according to an instruction from the information processing apparatus and for rendering off the first switch in response to the logical sum that is acquired by the OR means, and maintaining an OFF state until an instruction is received from the information processing apparatus, a second switch that is employed for connection and disconnection of the second power line, second ON/OFF control means for rendering on the second switch according to an instruction from the information processing apparatus and for rendering off the second switch in response to the logical sum that is acquired by the OR means and maintaining an OFF state until an instruction is received from the information processing apparatus; and employs the OR means also to report the output to the information processing apparatus.

In a preferred example of the present invention, an input/output device controller, which permits an information processing apparatus to communicate with a detachable input/output device, comprises: an interface that is employed for data exchange with an input/output bus of the information processing apparatus, a register for temporarily holding part of a data group that is to be exchanged, a driver for transmitting a signal to the input/output device, a power enabler for, in consonance with the contents written in the register, connecting/disconnecting a power line that joins the input/output device to a power source, detection means for detecting an over current across the power line, holding means for holding a detection result until an instruction is received from the information processing apparatus; and renders off the driver in response to an output of the holding means.

In another preferred example of the present invention, an input/output device controller, which permits an information processing apparatus to communicate with a detachable input/output device, comprises: an inter-

face that is employed for data exchange with an input/output bus of the information processing apparatus, a register for temporarily holding part of a data group that is to be exchanged, a driver for transmitting a signal to the input/output device, a power enabler for, in consonance with the contents written in the register, connecting/disconnecting a power line that connects the input/output device to a power source, detection means for detecting an over current across the power line, holding means for holding detection result until an instruction is received from the information processing apparatus; and provides in the register a field in which the detection result is written and renders off the driver in response to an output of the holding means.

Preferred embodiments of the present invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

Fig. 1 is a schematic diagram illustrating the hardware arrangement in the vicinity of a PCMCIA PC card slot according to a first embodiment of the present invention;

Fig. 2 is a graph showing a current that flows across power lines 35 and 36 when an over current detection result is not retained;

Fig. 3 is a diagram showing the detailed structure of a power controller 30 according to the first embodiment of the present invention, and more specifically, is a diagram showing the internal structure of the power controller 30 that can maintain the cut-off states of the power lines 35 and 36;

Fig. 4 is a timing chart for the ON/OFF operation of a switch 31 when the power controller 30 shown in Fig. 3 is employed;

Fig. 5 is a diagram showing the internal arrangement of a PCMCIA controller 20 according to the first embodiment of the present invention;

Fig. 6 is a diagram illustrating the arrangement of a register 23 in the PCMCIA controller 20 according to the first embodiment of the present invention;

Fig. 7 is a schematic diagram illustrating the hardware arrangement in the vicinity of a PCMCIA PC card slot according to a second embodiment of the present invention;

Fig. 8 is a diagram showing the system structure of a personal computer (PC) that implements the present invention;

Fig. 9 is a flowchart for the operation of the PC that implements the present invention;

Fig. 10 is a diagram showing a notebook computer where a PC card slot is provided on the side of the computer body; and

Fig. 11 is a schematic diagram illustrating a conventional hardware arrangement 100 with which a PC communicates with a PC card 60 that conforms to the standards specified by PCMCIA/JEIDA.

Embodiments of the present invention will be described in the following articles:

A. Hardware arrangement of a first embodiment

B. Hardware arrangement of a second embodiment

C. System structure of a PC that implements the present invention

D. Operation of a PC that implements the present invention

A. Hardware arrangement of a first embodiment

Fig. 1 is a schematic diagram illustrating the hardware arrangement in a vicinity 100 of a PCMCIA PC card slot according to a first embodiment of the present invention. In Fig. 1, the same reference numbers as are used in Fig. 11 are used to denote corresponding or identical components, and sections that are unnecessary to the explanation are not described. There are three differences between the first embodiment and the prior art in Fig. 11. These will now be described in detail.

The first difference between the first embodiment and the prior art in Fig. 11 is that an over current detector 40 is provided instead of the fuses 33 and 34 on the power lines 35 and 36. The over current detector 40 detects an over current that flows across the power lines 35 and 36.

As is shown in Fig. 1, a resistor 41, which converts a current into a voltage, is inserted in series on the power line 35. The two ends of the resistor 41 are connected respectively to the non-inversion terminal and the inversion terminal of a differential amplifier 43. The differential amplifier 43 has its threshold value set at a voltage level that corresponds to an over current value that is to be detected. When an over current flows across the power line 35, the differential amplifier 43 is rendered on. Similarly, a resistor 42 is connected in series on the power line 36, and a difference in the potentials at the two ends of the resistor 42 is detected by a differential amplifier 44. Since the over current detector 40 is constituted by an analog device, the response is quick, and as soon as a PC card with a power abnormality or with a large power consumption is loaded into a slot 50, the power lines 35 and 36 can be cut off from the voltage V_{CC} and V_{PP}.

The second difference between this embodiment

and the prior art is that the two detection results by the above described over current detector 40 are fed back to the power controller 30.

As is shown in Fig. 1, the outputs of the differential amplifiers 43 and 44 are transmitted to an OR gate 39. The OR gate 39, which is a component for outputting a logical sum of these two inputs, forwards an output OCS (Over Currency Signal) in response to the detection of an over current across at least one of the power lines 35 and 36. The output OCS of the OR gate 39 is sent to switch ON/OFF controllers 37 and 38. The switch ON/OFF controller 37 receives not only an output signal OCS from the OR gate 39, but also a control signal V_{CC}_En from a power enabler 24 of a PCMCIA controller 20, and forwards a logical product of the low-level OCS (i.e., the over current undetected state) and the high-level V_{CC}_En (i.e., the enabled state of the power line 35) to the gate of a switch 31. The switch ON/OFF controller 38 receives not only an output signal OCS from the OR gate 39, but also a control signal V_{PP}_En from the power enabler 24 of the PCMCIA controller 20, and forwards a logical product of the low-level OCS (i.e., the over current undetected state) and the high-level V_{PP}_En (i.e., the enabled state of the power line 36) to the gate of a switch 32. The switches 31 and 32 are P-channel MOS FET switches. When the outputs of the ON/OFF controllers 37 and 38 are high, i.e., when the power lines 35 and 36 are in the enabled state and an over current is not detected yet, the power lines 35 and 36 are connected to the respective power sources V_{CC} and V_{PP}. They are cut off in response to the detection of an over current. The cutoff of the power lines 35 and 36 is performed as a normal operation of the transistors 31 and 32 instead of by the destruction of components, such as fuses. Therefore, the replacement of such components as fuses, as is described in the [Description of the Background], is not required. The operation is started naturally by inserting a normal PC card.

Although, for simplifying the explanation, the switch ON/OFF controllers 37 and 38 have been employed simply as a combination circuit, such as an AND gate, it is preferable that the controllers 37 and 38 act as a sequence circuit that can latch the internal state. More specifically, it is desirable that, once an over current is detected, the OFF states of the switches 31 and 32 can be maintained at least until being reset by the insertion of another PC card. Since an over current is not detected by cutting off the switches 31 and 32, the closing and the opening of the switches 31 and 32 will be endlessly repeated if the over current detection result cannot be latched. As a result, a ringing current (a triangular wave current that has as its main amplitude a threshold value of the differential amplifiers 43 and 44), as is shown in Fig. 2, will flow across the power lines 35 and 36 (a ringing current will cause the thermal destruction of the PC card 60 and the slot 50 and is a waste of power for the PC). Fig. 3 is a detailed diagram for the internal structure of the power controller 30 that can latch the over current detection result. In Fig. 3, the ON/OFF controller 37 includes a NAND gate 37A, an SR latch 37B, and a pulse generator 37C, while the ON/OFF controller 38 includes a NAND gate 38A, an SR latch 38B, and a pulse generator 38C. Since the structures and the processing of the ON/OFF controller 37 and 38 are almost identical, an explanation will be given only for the ON/OFF controller 37. Signal V_{CC}_En from the power enabler 24 is directly input to one terminal of the NAND gate 37A, and is also input to the S terminal of the SR latch 37B via the pulse generator 37C. The output Q of the SR latch 37B is input to the other terminal of the NAND gate 37A. The NAND gate 37A inverts the logical product of the two inputs and outputs the result to the gate of the switch 31. The pulse generator 37C outputs one pulse each time an input signal goes high, and upon the receipt of one pulse at the S terminal, the SR latch 37B sets the output Q high (well known). When the signal V_{CC}_En is enabled, both inputs to the NAND gate 37A are high, and the switch 31 is turned on. The over current detection results for the power lines 35 and 36 are sent to the OR gate 39A, and then to the R terminal of the SR latch 37B via a pulse generator 39B. Upon the receipt of one pulse at the R terminal, the SR latch 37B resets the output Q (well known). Therefore, when an over current is detected for at least one of the power lines 35 and 36, the pulse generator 39B outputs one pulse, and the output Q of the SR latch 37B is set to low. Even when the V_{CC}_En is enabled, the output of the NAND gate 37A is set to high. As a result, the P-channel MOS FET switch 31 is turned off and maintained in the OFF state.

Fig. 4 is a timing chart for the ON/OFF operation of the switch 31 when the power controller 30 shown in Fig. 3 is employed. As is shown in Fig. 4, in response to the enabled state of V_{CC}_En, one pulse is input to the S terminal and the SR latch 37B is set. As a result, the switch 31 is also turned on. When an over current is detected, one pulse is input to the R terminal, and the SR latch 37B is reset. As a result, the switch 31 is also turned off. It would be understood by one having ordinary skill in the art that once an over current is detected, the switch 31 is maintained in the OFF state even when V_{CC}_En is enabled.

The third difference between the first embodiment and the prior art is that the two outputs of the over current detector 40 are fed back to the PCMCIA controller 20. More specifically, the output of the OR gate 39 is individually sent to the driver 25 and the register 23.

Fig. 5 is a diagram showing an essential internal structure of the PCMCIA controller 20, which is required for the explanation, according to the first embodiment of the present invention. As is shown in Fig. 5, the output of the OR gate 39A, which is the over current detection result for the power line 35 or 36, is also sent to a latch 39C. The latch 39C is a sequence circuit that maintains its output OCS high when a high output is received from the OR gate 39A, and is implemented by a D latch, for example. The output of the latch 39C is forwarded to the

register 23 and the driver 25. Upon the receipt of the high level signal OCS, the register 23 writes an OCS bit at a predetermined address, which will be described later. The driver 25, which is an equivalent circuit to a buffer for transmitting power, receives the inverted OCS signal at a gate control terminal of the buffer. Therefore, in response to the high OCS signal that is accompanied by the over current detection, the driver 25 falls into a high impedance state (Hi-Z), and as a result, the transmission of a bus signal to the PC card 60 can be halted.

Fig. 6 is a diagram showing a part of the internal structure of the register 23 of the PCMCIA controller 20. In Fig. 6, address k points to an input register in which a V_{CC} bit and a V_{PP} bit, instructions for supplying power to the power lines 35 and 36, are written. Address m points to an output register in which an event indicator (Card Detect) for the loading of the PC card 60 to the slot 50 is written. Address n points to an output register in which an event indicator (OCS bit) for the detection of an over current is written, and to which a detection signal OCS is input (previously described). The register 23 is generally arranged by referring to Intel 182365SL, while the output register in which the contents of the OCS bit are written is unique to this embodiment. Since the PC can access the register 23 during a normal I/O read cycle, a PC card power abnormality can be found by the reading data at address n. Although the register 23 includes many other I/O registers, they are well known to one having ordinary skill in the art and no explanation for them will be given.

B. Hardware arrangement of a second embodiment

Fig. 7 is a schematic diagram illustrating the hardware arrangement for a vicinity 100 of a PCMCIA PC card slot according to a second embodiment of the present invention. In Fig. 7, the same reference numbers as are used in Fig. 11 are used to denote corresponding or identical components. Sections that are not required for the explanation are not shown in Fig. 7.

In the second embodiment, instead of the over current detector 40, fuses 31 and 32 are employed as in the prior art (Fig. 11) to cut off power at power lines 35 and 36. It should be noted that this embodiment differs from the prior art in that the power cutoff by the fuses 31 and 32 is fed back to a PCMCIA controller 20.

In Fig. 7, the emitter of a pnp transistor Q1 is connected to the power V_{CC} side terminal of a fuse 33, and its base is connected to the PC card 60 side terminal of the fuse 33 via a resistor R_1. Since the base and the emitter have the same electric potential while the fuse 33 is coupled, the transistor Q1 is rendered off. When an over current flows across the power line 35 and the fuse 33 blows, the base is pulled down to the GND with the PC card 60 as a load, and a bias voltage V_{CC} is applied to the emitter. The transistor Q1 is rendered on and is maintained in this state. The emitter of the transistor Q2, which is also a pnp transistor, is connected to the voltage V_{PP} side terminal of a fuse 34 and its base is connected to the PC card 60 side terminal of the fuse 34 via a resistor R_2. Although the transistor Q2 is rendered off when the fuse 34 is coupled, once the fuse 34 blows, the transistor Q2 is rendered on and is maintained in this state.

The collector terminals of the transistors Q1 and Q2 are OR-coupled at point S and are then branched. One end is connected to the base of an npn transistor Q3 via a resistor R_4, and the other end is pulled down to the GND via a resistor R_5. The emitter of the transistor Q3 is pulled down to the GND, and a system voltage V_{DD} is applied to the collector of the transistor Q3 via a resistor R_3. Since the base potential is maintained as a GND level as long as a normal current flows across the power lines 35 and 36 and the transistors Q1 and Q2 are rendered off, the transistor Q3 is also rendered off and a voltage at point T is kept high. When an over current flows across at least one of the power lines 35 and 36, either transistor Q1 or Q2, or both, are rendered on, and in response to this a current flows to the base. Thus, the transistor Q3 is rendered on and maintained in the ON state. Further, a current flows from the collector of the transistor Q3 to its emitter and a voltage at point T drops to low.

The collector terminal of the transistor Q3 is branched at point T. A signal, FBO (Fuse Blow Out), which reports the blowing of the fuses 33 and 34, is carried over one of the branched signal lines and through an inversion buffer B. The signal FBO is transmitted to address n of the register 23 and to the gate control terminal of the driver 25 in the PCMCIA controller 20. When both the fuses 33 and 34 are coupled, the FBO, which is the inversion signal for the collector of the transistor Q3, is maintained low. When at least one of the fuses 33 and 34 has blown, the signal FBO goes high and is maintained high. Since hereafter a high potential voltage is applied to the gate control terminal of the driver 25, and the driver 25 goes into a high impedance state, a bus signal can not be output. In response to the high level signal FBO, an OCS bit indicating that the power is cut off is set at address n in the register 23. The structures and the operational characteristics of the register 23 and the driver 25 are the same as those in the first embodiment.

Since the high-level signal FBO can be maintained by the blowing of the fuses 33 and 34, the latch 39C shown in Fig. 5 is not necessary. The resistors R_1, R_2, R_3, R_4, and R_5 are components for voltage-current conversion and for current-voltage reconversion, and are approximately 1 kΩ to 10 kΩ.

C. System structure of a PC that implements the present invention

Fig. 8 is a schematic diagram illustrating the system structure of a PC that implements a PCMCIA PC card slot according to the first and the second embodiments

of the present invention.

The lower half tiers are hardware tiers and their details are as described in article A or B. For the PC card 60, besides memory card specifications, there are I/O card specifications, such as those for a fax/modem card, a LAN adaptor card, an HDD card, and an IR (infrared communication) adaptor card. The PC includes one or more slots into which a PC card is loaded.

The lowest tier level of software is a socket service. The socket service is PC card control software that includes a function call for directly accessing the PCMCIA controller 20 for control performance. More specifically, the socket service has functions such as the acquisition of the state of the PC card slot 50, the resetting of an interrupt level when the state of the slot 50 is changed, and the mapping of the memory and the I/O port of the PC card 60 to the PC.

A card service, which is PC card control software that is located between the socket service and upper system software, can issue a function call to the socket service. More specifically, the card service has a table for the hardware resources (e.g., memory space and I/O space that a PC card uses, and an interrupt level) that are assigned to each PC card. In response to the attachment and detachment of the PC card, the hardware resources can be actively re-distributed, and the PC card attachment and detachment events can be reported to a corresponding device drive or to a corresponding application program.

In the hardware control tiers, data are exchanged between individual hardware components of the system, and an ordinary command that is issued by the upper software is changed to operable code by the hardware and is transmitted to the lower tier. Device drivers for operating a fax/modem card, a LAN adaptor card, an HDD card, and a serial IR (Infrared communication) adaptor card are the equivalent of these hardware components. The device drivers can issue a function call to the card service for the assignment of hardware resources.

An operating system (OS) is the basic software for controlling the execution of the application programs at the highest tier level. More specifically, the operating system performs resource management, such as a command process, memory control, input/output control, and task management, to enable a PC to execute application programs, and also provides for a user an interface environment, such as a system command or a system call. OS/2 (U.S. IBM trademark) and AIX (U.S. IBM trademark) are the equivalents of such the operating system. The OS is sometimes equipped with standard device drivers, card services, and configuration software.

At the highest tier level are application programs, which are loaded by a user from an auxiliary storage device into a main memory. Since these are not associated with the subject of the present invention, a detailed explanation of them will not be given.

D. Operation of a PC that implements the present invention

Since the hardware and software arrangements of the system for implementing the present invention have been described, the operation of the system and the processing of the present invention will be explained in this article.

Fig. 9 is a flowchart for the operation when a PC card 60 is loaded into a PC that implements the present invention. The procedures at the individual steps will now be described in detail.

When the PC card 60 is inserted into the slot 50, the socket service detects and reports this via the card service to the device driver (step S12).

Then, the PC (more specifically, the device driver) tries to power on the PC card 60 by writing the V_{CC} bit and the V_{PP} bit at address k of the register 23 (step S14). When an over current across at least one of the power lines 35 and 36 is detected, or when one of the fuses has blown, the OCS bit is set in the register 23 (previously described). The socket service reads the contents at address n into the register 23 during the I/O read cycle (step S16). Then, a check is performed to determine whether or not the supply of power to the power lines 35 and 36 is normal (step S18).

If the decision at step S18 is affirmative, upon a request from the configuration software of the device driver, the socket service reads the attribute information for the PC card 60 (card information structure: CIS) (step S20). Then, the card service employs the CIS and actively redistributes the PC hardware resources, by assigning to the PC card 60 memory space and I/O space in the PC, and an interrupt level (step S22). Then, the PC is set in its normal operational state (step S24). The CIS comprises PC card identification information, access speed, electric specifications, and configuration, and is written into, for example, a ROM that is incorporated in the PC card 60.

When the decision at step S18 is negative, i.e., when the OCS bit is set at address n in the register 23, it is reported as error information to the OS via the socket service and the card service. The OS may report the contents of the error to a user via a GUI (Graphical User Interface) (step S26). Since the notice is reported to a user via the GUI, reoccurrence of a fault, such as insertion of the PC card 60 into other slots, can be prevented. The insertion of the PC card 60 is abnormally terminated (abort), and later access to the PC card 60 may be inhibited (step S28).

The present invention has been explained in detail while referring to the specific embodiment. It will be obvious, however, to one having ordinary skill in the art that the above embodiment may be modified or varied without exceeding the scope of the present invention. In other words, while the present invention has been disclosed by using an example, it is not limited to this example. To understand the subject of the present inven-

tion, claims should be referred to.

As described above in detail, according to the present invention, it is possible to provide a power enabling mechanism, a power enabling method, and an input/output device controller for securely supplying power to a PC card that is loaded into a slot of a personal computer (PC), and for preventing a voltage reduction and circuit fault of the PC and the latch-up of the PC card even when power consumption by the PC card is abnormal (or a large power consumption exceeds specified standards).

More specifically, according to the present invention, even when, among the two system power lines for V_{CC} and V_{PP} that are specified by PCMCIA, only the power line for the referential voltage V_{CC} is cut off, the power line for V_{PP} can also be cut off, and the undesired destruction of the PC card can be prevented.

Further, according to the present invention, when an abnormality is detected in the supply of power to the PC card, the detection result can be reported to the PC. Therefore, as the result can also be reported to a user via a GUI (Graphical User Interface), etc., no unnecessary effort to confirm an abnormality is required.

In addition, according to the present invention, when an abnormality is detected in the supply of power to the PC card, the output of the driver for transmitting a signal (an address signal, data signal, or a control signal) to the PC card is halted, and the destruction of the internal circuit of the PC card due to the latch-up, etc., can be prevented.

Moreover, according to the present invention, when a PC card that has a power supply abnormality is loaded into a card slot, the power line cut-off and/or the output halt of a bus signal to the PC card can be maintained. Therefore, even when a PC card that has an abnormality is being loaded, ringing of a supplied current that accompanies the repetitious connection and disconnection of the power lines to the power source can be prevented.

Claims

1. Apparatus for controlling a supply of power by an information processing system to a detachable input/output device, comprising:

   a first power line for supplying power at a first voltage level;

   a second power line for supplying power at a second voltage level;

   a first detector for detecting an over current across the first power line;

   a second detector for detecting an over current across the second power line;

   OR means for logically adding the outputs of both the first and second detectors;

   a first switch that is employed for connection and disconnection of the first power line in response to an output of the OR means; and

   a second switch that is employed for connection and disconnection of the second power line in response to an output of the OR means.

2. Apparatus as claimed in claim 1, wherein the OR means also to report the output to the information processing apparatus.

3. Apparatus as claimed in claim 1 or 2, wherein the first and the second switches are constituted by a MOS FET transistor or a bipolar transistor.

4. Apparatus as claimed in any preceding claim, wherein:

   the first detector comprises a first fuse that blows when an over current flows across the first power line, and a first detection line that is set to the ON state by the blowing of the first fuse;

   the second detector comprises a second fuse that blows when an over current flows across the second power line; and

   a second detection line that is set to the ON state by the blowing of the second fuse; and

   the OR means comprises a report line that is employed to carry a notice to the information processing apparatus when at least one of the first and the second detection lines is set in the ON state.

5. Apparatus as claimed in claim 1, 2, or 4, wherein the detachable input/output device is a PC card that conforms to standards specified by PCMCIA/JEIDA.

6. An input/output device controller, which permits an information processing apparatus to communicate with a detachable input/output device, comprising:

   an interface that is employed for data exchange with an input/output bus of the information processing apparatus, a register for temporarily holding part of a data group that is to be exchanged,

   a driver for transmitting a signal to the input/output device,

a power enabler for, in accordance with data that are written into the register, connecting/disconnecting a power line that joins the input/output device to a power source, detection means for detecting an over current across the power line; and

rendering off the driver in response to the detection result that is obtained by the detection means.

7. An input/output device controller as claimed in claim 6, wherein the driver is rendered off when the driver enters the high state.

8. A power enabling method, for controlling a supply of power by an information processing apparatus to a detachable input/output device, comprising the steps of:

detecting whether or not there exists a supplied power abnormality; halting the supply of power in response to detection of the abnormality;

halting transmission of a signal to the input/output device in response to the detection of the abnormality; and

reporting the detection of the abnormality to the information processing apparatus.

9. A method as claimed in claim 8 comprising the step of:

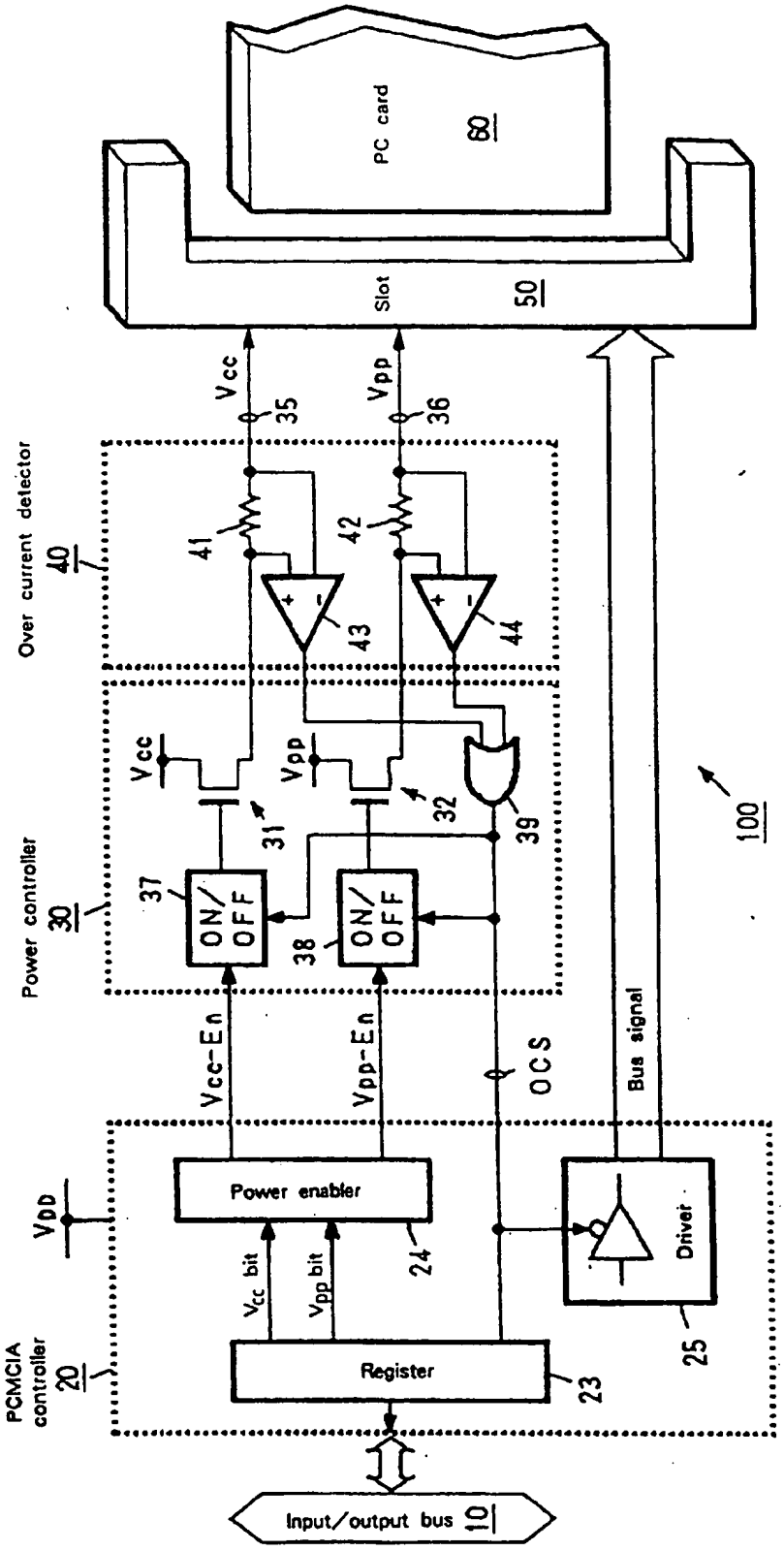
maintaining the halting of the supply of power to the input/output device at least while the input/output device is loaded.

10. Apparatus as claimed in claim 1 or claim 2 comprising:

first ON/OFF control means for rendering on the first switch according to an instruction from the information processing apparatus and for rendering off the first switch in response to the logical sum that is acquired by the OR means and maintaining an OFF state until an instruction is received from the information processing apparatus;

second ON/OFF control means for rendering on the second switch according to an instruction from the information processing apparatus and for rendering off the second switch in response to the logical sum that is acquired by the OR means and maintaining an OFF state until an instruction is received from the information processing apparatus.

FIG. 1


PC card
60
Slot
50
Vcc
Vpp
35
36
Over current detector
40
41
42
43
44
Power controller
30
31
32
37
38
39
ON/OFF
100
Vcc-En
Vpp-En
OCS
Bus signal
Power enabler
Driver
VDD
Vcc bit
Vpp bit
24
25
PCMCIA controller
20
Register
23
Input/output bus 10

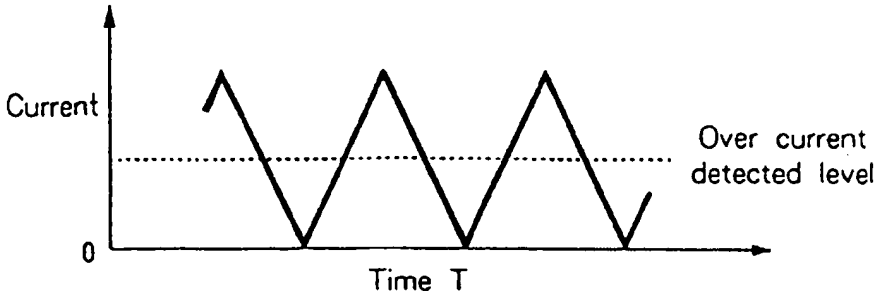

Current
Over current
detected level
0
Time T

FIG. 2

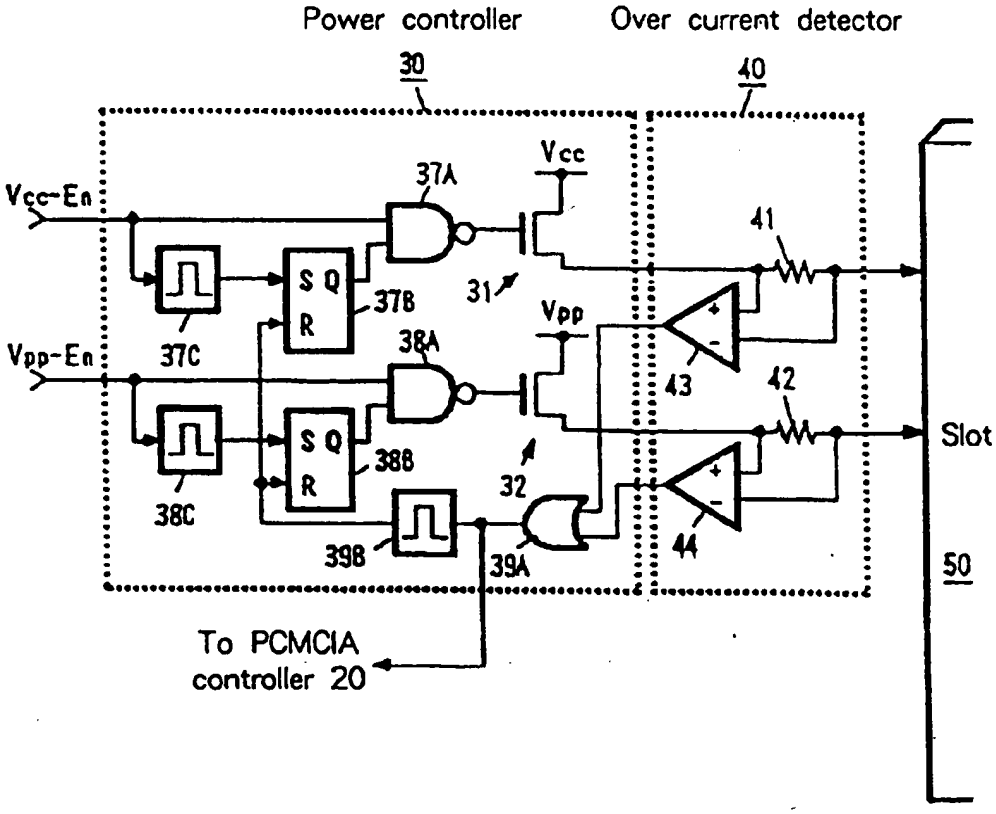

Power controller
Over current detector
30
40
Vcc
Vcc-En
37A
41
S Q
R
37B
31
37C
Vpp
Vpp-En
38A
43
42
Slot
38C
38B
32
39B
39A
44
50
To PCMCIA
controller 20

FIG. 3

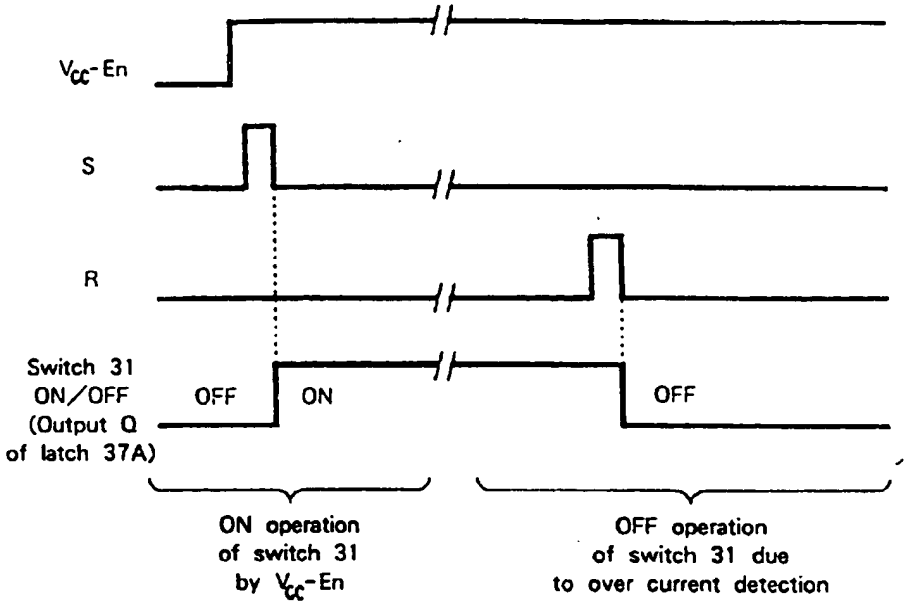

V_{CC}-En
S
R
Switch 31
ON/OFF
(Output Q
of latch 37A)
OFF
ON
OFF
ON operation
of switch 31
by V_{CC}-En
OFF operation
of switch 31 due
to over current detection

FIG. 4

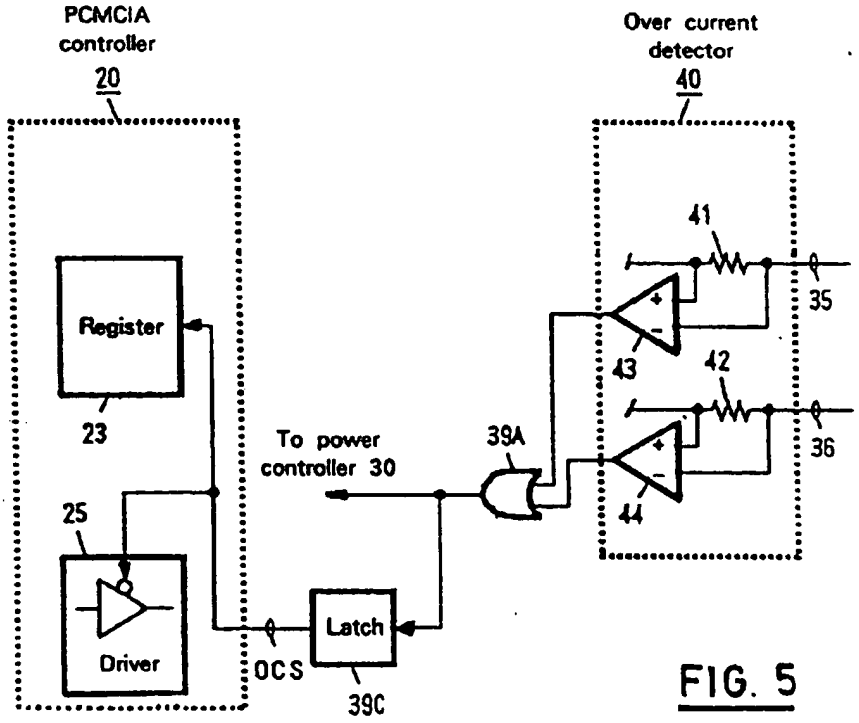

PCMCIA
controller
20
Over current
detector
40
Register
23
25
Driver
To power
controller 30
39A
Latch
OCS
39C
41
35
43
42
36
44

FIG. 5

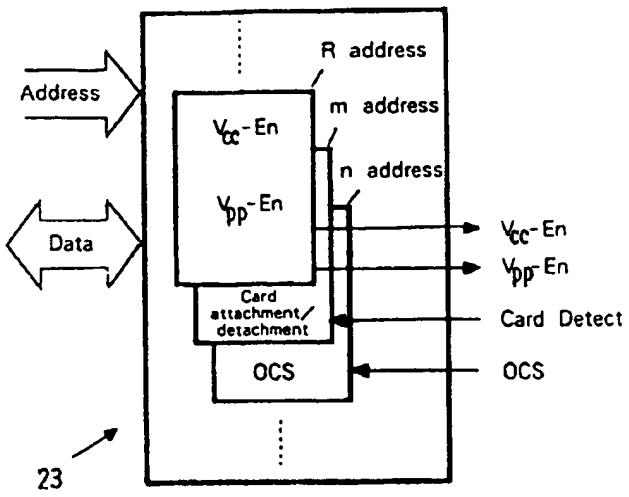

Address
Data
R address
m address
n address
V_{cc}-En
V_{pp}-En
Card attachment/ detachment
OCS
V_{cc}-En
V_{pp}-En
Card Detect
OCS
23

FIG. 6

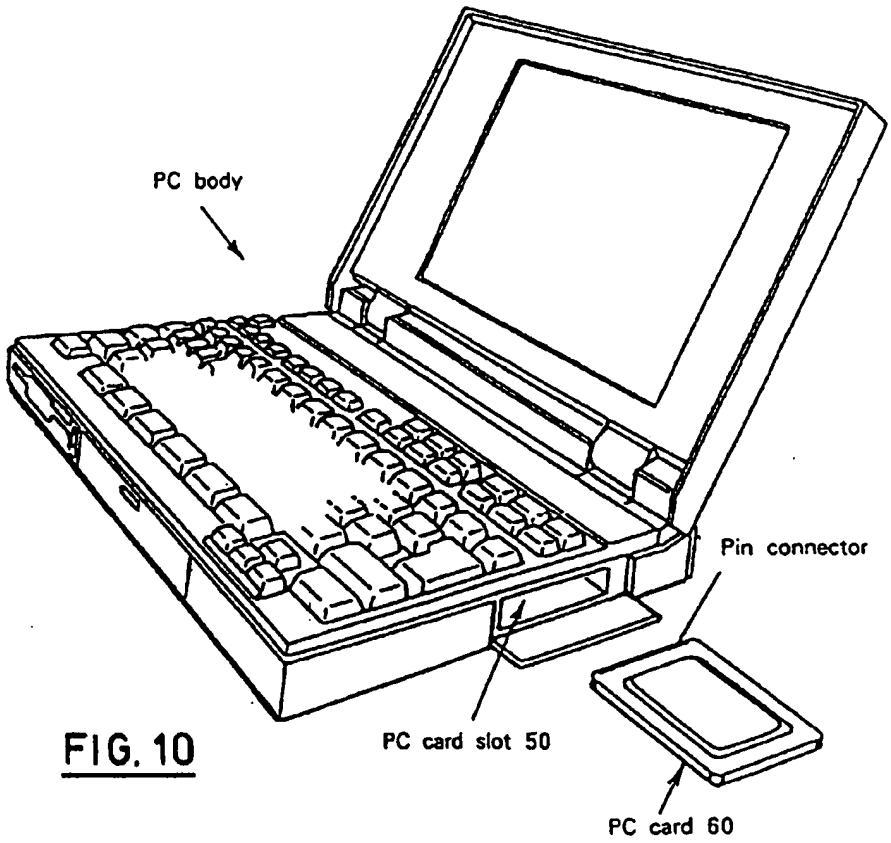

PC body
Pin connector
PC card slot 50
PC card 60

FIG. 10

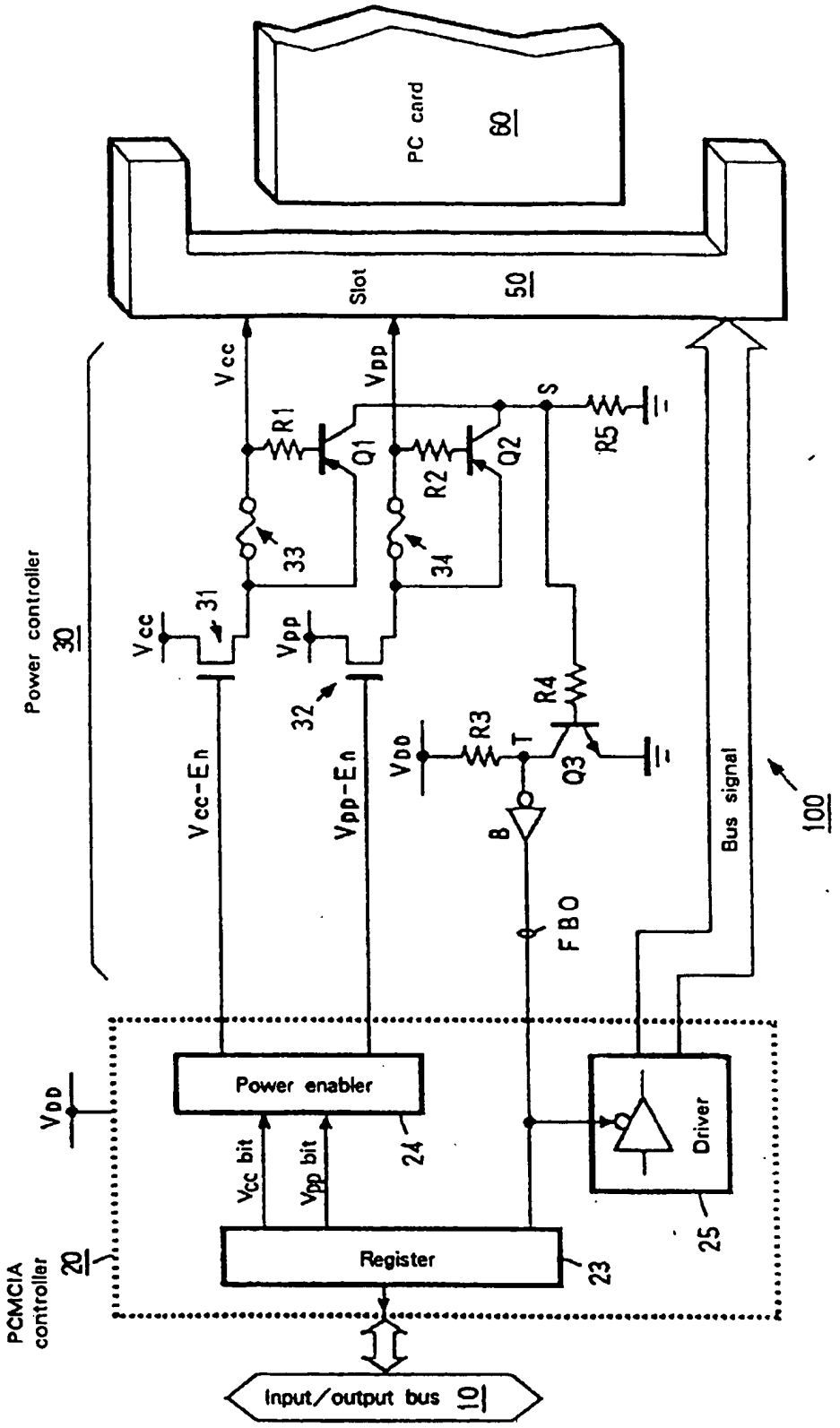

PC card
60
Slot
50
Vcc
Vpp
S
R1
Q1
R2
Q2
R5
33
34
31
Vcc
Vpp
32
R4
R3
T
Q3
VDD
Power controller
30
Vcc-En
Vpp-En
B
FBO
Bus signal
100
Power enabler
24
Driver
25
VDD
Vcc bit
Vpp bit
Register
23
PCMCIA controller
20
Input/output bus 10

FIG. 7

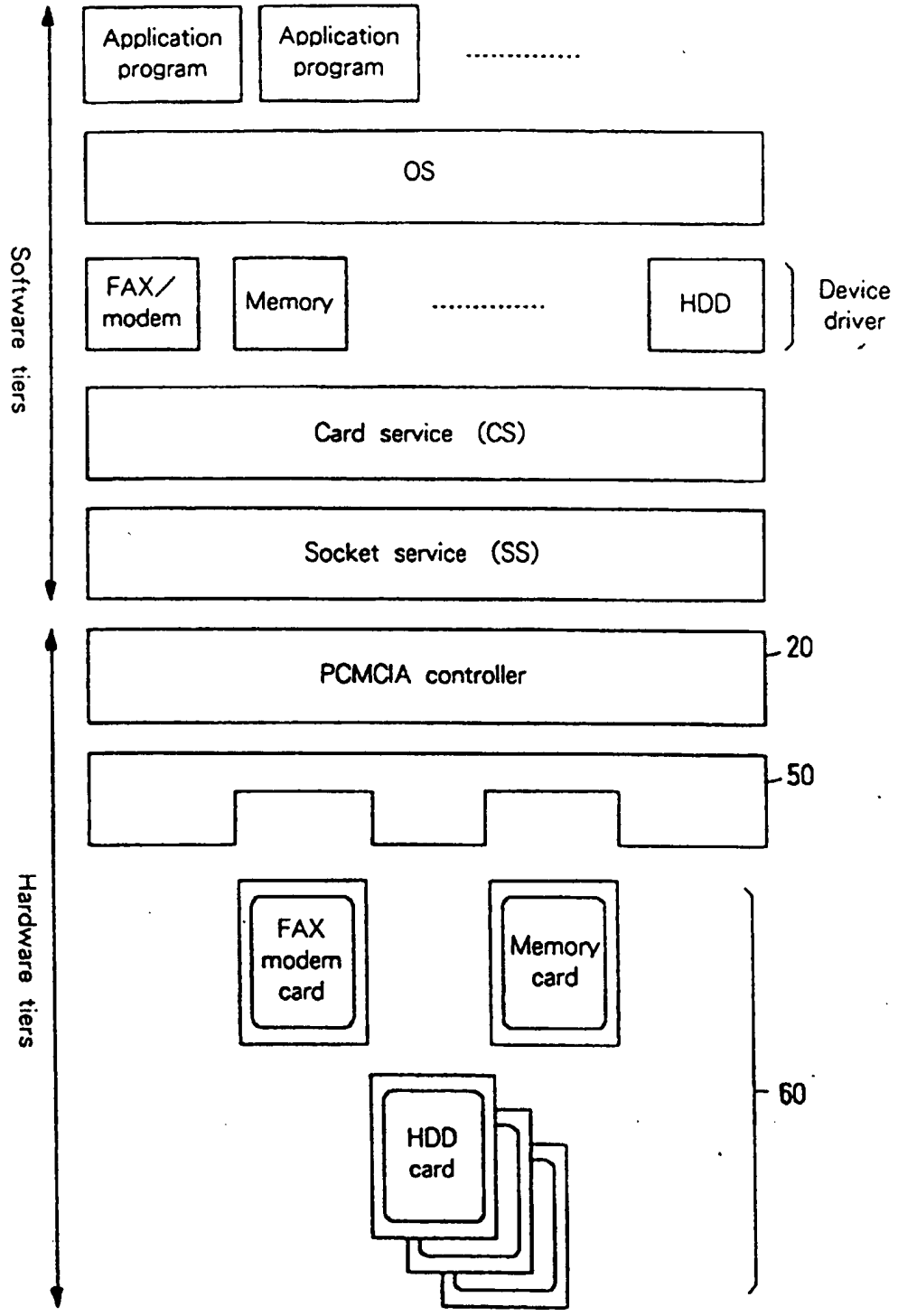

Application program
Application program
.....
OS
FAX/ modem
Memory
.....
HDD
Device driver
Card service (CS)
Socket service (SS)
Software tiers
PCMCIA controller
20
50
FAX modem card
Memory card
HDD card
60
Hardware tiers

FIG. 8

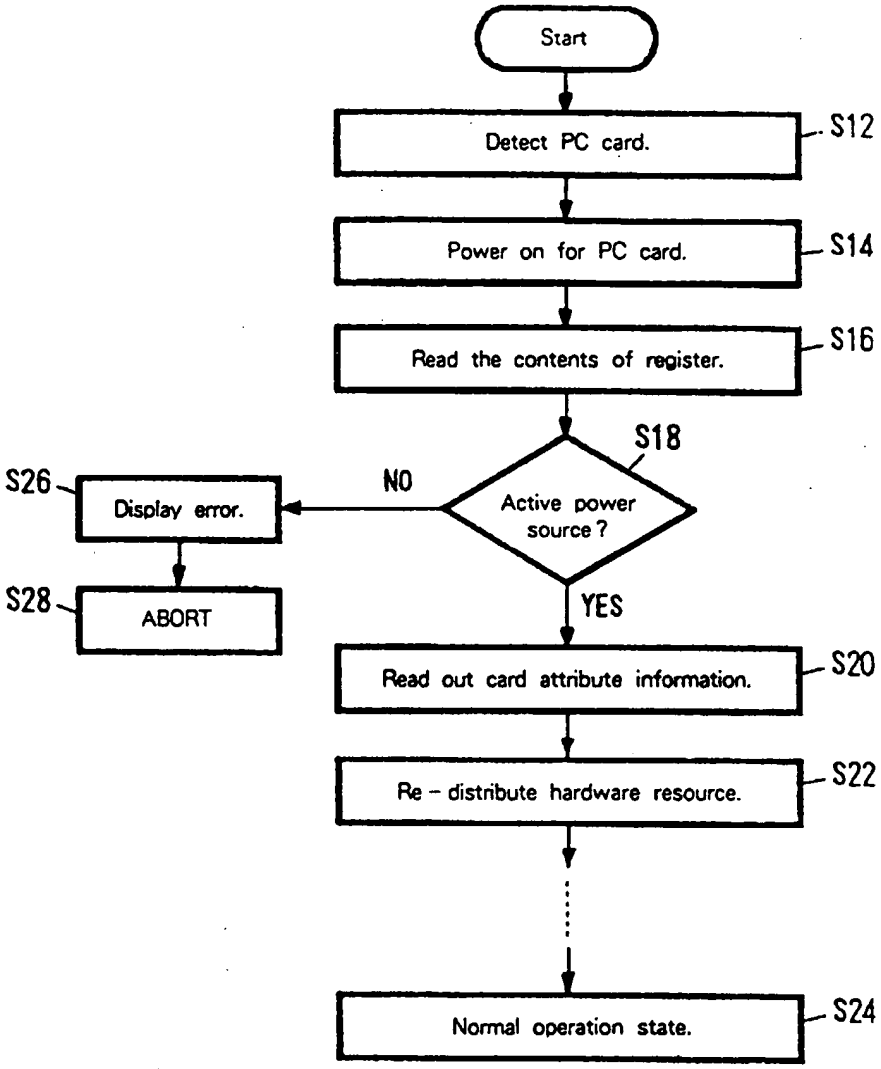
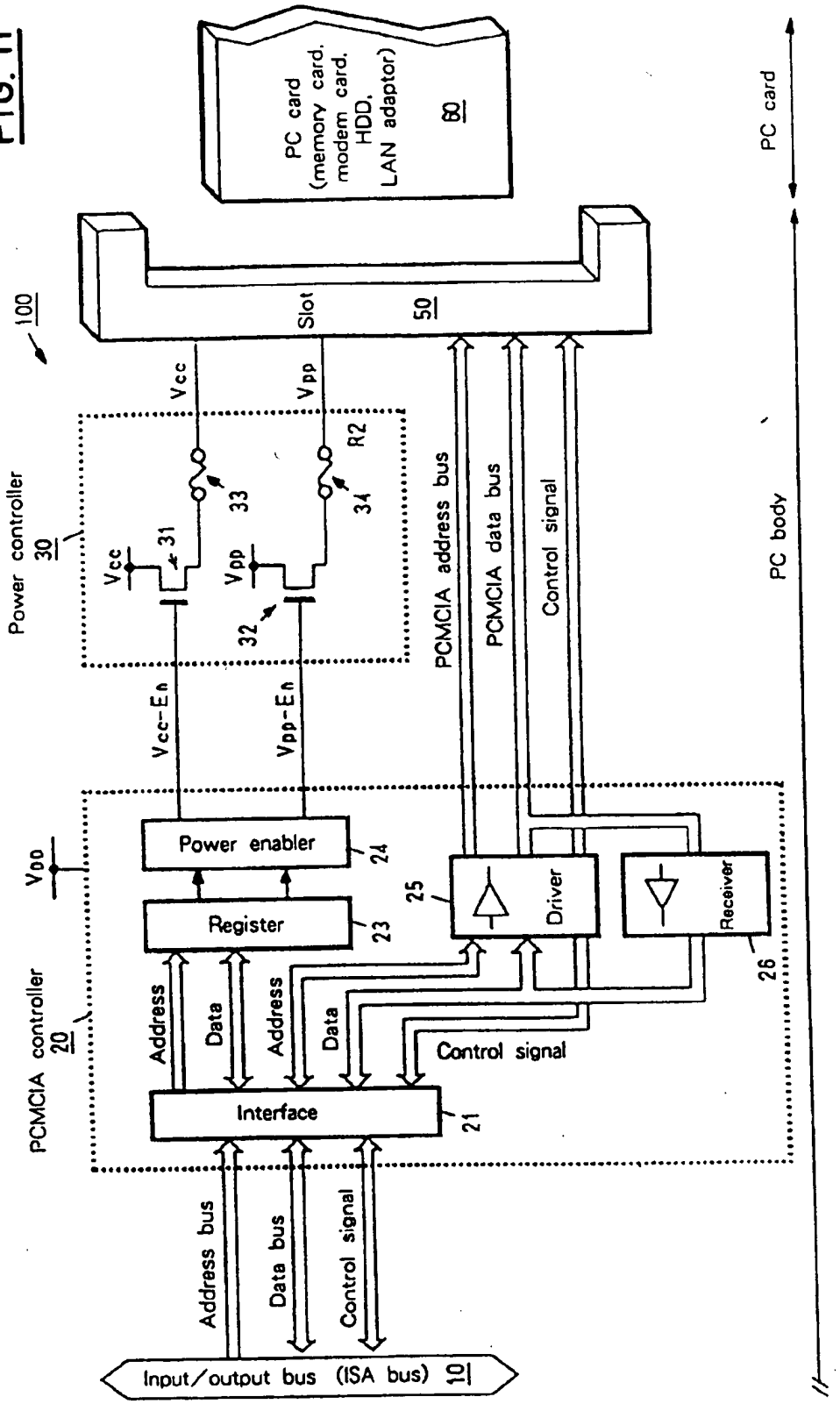

Start
Detect PC card.
S12
Power on for PC card.
S14
Read the contents of register.
S16
S18
Active power source ?
NO
S26
Display error.
S28
ABORT
YES
Read out card attribute information.
S20
Re - distribute hardware resource.
S22
Normal operation state.
S24

FIG. 9

FIG. 11


PC card
(memory card.
modem card.
HDD.
LAN adaptor)
80
PC card
100
Slot
50
Vcc
Vpp
R2
Power controller
30
Vcc
31
33
Vpp
34
32
PCMCIA address bus
PCMCIA data bus
Control signal
PC body
Vcc-En
Vpp-En
Power enabler
24
VDD
Register
23
25
Driver
Receiver
26
PCMCIA controller
20
Address
Data
Address
Data
Control signal
Interface
21
Address bus
Data bus
Control signal
Input/output bus (ISA bus) 10

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 30 8416

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP-A-0 363 871 (OKI ELECTRIC IND CO LTD) 18 April 1990 * column 3, line 18 - line 25 * * column 4, line 21 - column 6, line 37 *	1,3,5,8, 9	G06F1/26 G06K7/00
Y		2,6,7	

Y	US-A-4 964 011 (STERNGLASS DANIEL) 16 October 1990 * column 3, line 52 - column 5, line 8; figure 3 *	6,7	
A		8	

Y	EP-A-0 063 611 (FANUC LTD) 3 November 1982 * column 6, line 5 - line 22 * * column 7, line 7 - column 8, line 22 *	2	
A		1,4,8	

A	ELECTRONIC DESIGN, vol. 42, no. 18, 5 September 1994 page 47/48, 50, 52 XP 000475986 GOODENOUGH F 'HOST CPU'S IC MANAGES POWER FOR PCMCIA CARDS' * page 52, left column, line 13 - right column, line 10 *	3-6,8	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)
G06F
G11C
G06K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	27 March 1996	Bailas, A

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)